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REVIEW ARTICLE

Challenges and Progress in the Fabrication of Silicon Nanowire Tunnel Diodes

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Abstract

Tunnel (Esaki) diodes prepared in silicon (Si) nanowires could provide a unique platform to investigate band-to-band tunneling (BTBT) transport in nanoscale. However, the successful fabrication of these devices poses substantial challenges, related to controlling high doping concentrations, maintaining the abruptness of the *pn* junction, and minimizing roughness due to nanoscale patterning. This paper comprehensively addresses these challenges, suggesting potential strategies for optimization. Additionally, examples of nanoscale diodes fabricated so far in silicon-on-insulator (SOI) substrates are showcased, highlighting their tunnel-diode characteristics at low temperatures. Furthermore, the underlying physics is discussed: phonon-assisted tunneling, single-charge tunneling and donor-acceptor compensation. For practical applications, such as photodetectors or tunnel field-effect transistors, room-temperature operation is also required.

Keywords: silicon, nanowire, pn diode, band-to-band tunneling, silicon-on-insulator, nanofabrication

1. Introduction

Tunnel (Esaki) diodes are the first semiconductor devices in which quantum-mechanical tunneling has been demonstrated [1, 2] as band-to-band tunneling (BTBT). Immediately after this discovery, there was significant research in the 1950s and 1960s on phonon-assisted BTBT, role of gap states in the excess current and the analysis of the negative differential conductance (NDC) peak, which is a specific property of these devices [3, 4, 5]. However, the research stagnated until recently, when the interest in BTBT transport increased due to the emergence of the tunnel field-effect transistors (TFETs) [6, 7]. These devices operate specifically by BTBT and promise

subthreshold slopes smaller than the conventional metal-oxide-semiconductor field-effect transistors (MOSFETs). As a consequence, research on BTBT transport has been recently accelerated, especially focusing on BTBT in nanowire devices [8]. Esaki diodes fabricated with nanowires grown to have dimensions on the order of 100 nm were reported to still operate as classical Esaki diodes, so further reduction of the dimensions is needed to unlock nanoscale-specific characteristics. In this direction, developing CMOS-compatible processes for fabrication of such nanoscale tunnel diodes can allow a high-quality interface and an advanced control of the parameters, opening doors to a diverse range of applications.

In this work, we highlight remaining challenges in the fabrication of nanoscale silicon (Si) tunnel diodes, as depicted in Fig. 1. These challenges include attaining high doping concentrations, maintaining junction abruptness, and controlling the surface roughness due to nano-patterning. Even with these challenges not fully solved, tunnel diodes fabricated so far in silicon-on-insulator (SOI) films exhibit already phenomena that are of interest in terms of physics, as will be illustrated in the latter part.

2. Challenges of Tunnel-Diode Nanofabrication

Based on the background presented above, a few main challenges are presented one by one in the following sections. These challenges must be well understood and overcome in order to form abrupt, nanoscale depletion layers in high-quality tunnel diodes for the observation and application of the BTBT transport mechanism.

2.1 Reaching High Enough Doping Concentrations

Doping is the key process used to change the conductivity of Si by introducing substitutional impurities, specifically phosphorus (P) donors and, respectively, boron (B) acceptors, forming *n*-type and, respectively, *p*-type regions. Doping is typically carried out in a two-step process (pre-deposition and drive-in), with the drive-in temperature and time mostly dictating the doping level. A limiting factor is the solid solubility of the dopants in Si, which depends on the temperature and doping conditions, but generally is on the order of $5 \times 10^{20} cm^{-3}$ [9]. For instance, for a drive-in temperature of $950^{o}C$, solid solubility is $7.8 \times 10^{20} cm^{-3}$ for P in Si, but only $3.9 \times 10^{20} cm^{-3}$ for B in Si [9, 10].

In order to maintain the crystallinity of the doped Si, the drive-in temperature should also be limited to much lower than the melting temperature of Si ($1410^{o}C$). In our case, the drive-in temperature is limited in the range 850 $1050^{o}C$.

It should also be noted that, in order to minimize roughness due to direct contact of the doping source with Si, a thin (1.0 ± 0.2 nm) SiO_2 film is thermally grown before doping. Despite preserving the surface quality, this film also acts as a diffusion barrier for doping, further limiting the incorporation of dopants into the Si lattice.

Due to the above reasons, typical doping concentrations that can be reached by our regular process are in the range 0.5 $2.5 \times 10^{20} cm^{-3}$, with ND usually larger than NA. These values are still large enough (higher than the metal-insulator transition concentration for Si, $NMIT \approx 3.8 \times 10^{18} cm^{-3}$) to ensure that the Fermi levels are within the respective bands, for a few tens of meV [11]. However, for electrical measurements taken at low temperatures (5-10 K), as the cases presented in this work,

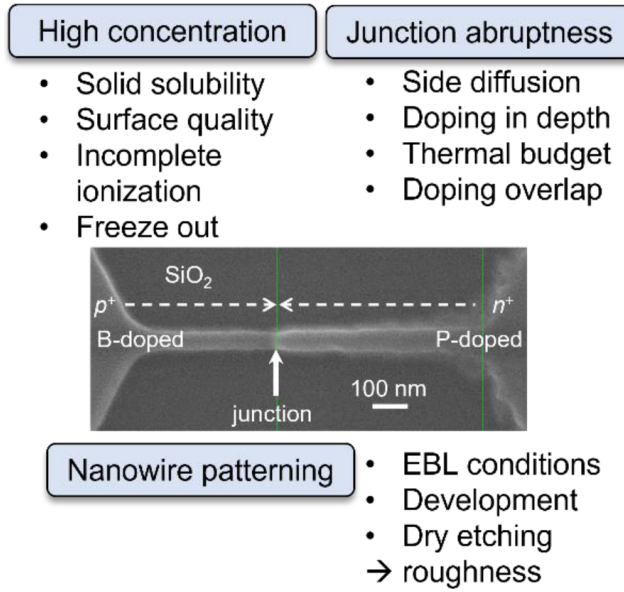

Figure 1. An overview of issues related to the fabrication of nanoscale lateral p^+n^+ SOI diodes. An SEM image in the center shows the nanostructure patterned by EBL, after being doped with B-acceptors (p^+) and with P-donors (n^+). Issues may arise due to the need to attain high doping concentrations, maintain junction abruptness and achieve nanowire patterning.

freeze-out effect should also be taken into account [12]. Freeze-out effect consists in a significant reduction of the free-carrier concentration due to trapping of carriers in the dopants. In addition, it is actually well known that incomplete ionization occurs also at higher temperatures, even at room temperature [13, 14].

Finally, it should be noted that the fabrication of *pn* nanodevices is completed by forming a passivating oxide layer (at least partly by thermal oxidation). In such case, it is known that some of the dopants (usually, B-acceptors) tend to diffuse into the SiO_2 layer as this is grown into Si [15]. This is another factor in the reduction of doping concentration from the designed value.

The factors described above must be well understood and controlled for the realization of highly-doped *pn* diodes (i.e., p^+n^+ tunnel diodes), with sufficiently narrow depletion layers. Some of the factors (such as freeze out or incomplete ionization) can be removed simply by raising the temperature of the measurements. The demerit of high-temperature operation is, however, that thermally-activated current is enhanced, which disturbs the observation of pure BTBT current. Other factors (such as the surface quality) can be mitigated by further optimization of the device processing, e.g., by rapid thermal annealing (RTA) with increased control.

2.2 Maintaining Abruptness of the pn Junction

Effective BTBT transport can be observed when the depletion layer has its main dimension (width) on the order of 10 nm or less. This implies not only high doping

concentrations, N_D and N_A, but also abruptness of the *pn* junction. For a graded *pn* junction, the condition $N_D \approx N_A$ holds approximately for a longer distance across the junction, which enhances the effect of compensation between dopants of opposite polarities. An extension of the depletion layer and a weaker built-in electric field are expected in this case [16]. Since BTBT depends exponentially on the tunnel barrier (in this case, depletion-layer width), the BTBT current level becomes significantly reduced with any increase of the depletion layer.

It is beneficial, therefore, to preserve the abruptness of the *pn* junction while keeping also N_D and N_A high [17]. However, these issues are often conflicting with each other, and a compromise must be reached. Leveraging rapid thermal annealing (RTA), one can reduce the drive-in time to the order of only several tens of seconds, which can limit side diffusion in a lateral *pn*-diode design. On the other hand, such limited drive-in time may result in shallower dopant diffusion. Subsequent processing steps for device fabrication can make this issue a critical one. In addition, doping must be done sequentially (typically, first with P-donors and then with B-acceptors), but the thermal budget of the second doping step will also affect the dopants introduced in the first step. Similarly, the thermal oxidation at the end of processing will also contribute to side diffusion of both types of dopants. These factors are also listed in Fig. 1.

In a recent process used to create such devices, an overlap is introduced between the doping with P-donors and B-acceptors, to ensure that the junction is formed within the nanostructures [18, 19]. In that case, the *pn* junction location and width will be mostly dictated by one of N_D or N_A (whichever is larger) and by the abruptness of its decay near the doping-mask edge. Further optimization is needed by using ultra-short-time RTA and making the Si layers much thinner at the stage of doping, which may provide a solution for achieving abrupt p^+n^+ tunnel diodes.

2.3 Nanoscale Patterning and Roughness Control

Although doping concentration and abruptness of the doping profiles are critical for defining a narrow *pn* junction, the transport properties could be even more critically affected by roughness induced by nanoscale patterning. Therefore, it is essential to achieve control of dimensions in nanoscale and to preserve the flatness of the surfaces. Electron beam lithography (EBL) techniques, using thin resists that can be accurately developed and dry etching methods (such as reactive ion etching, RIE) can allow the formation of nanowires or nanosheets, with dimensions in the range of 10–100 nm. An example is shown by an SEM image in Fig. 1. However, roughness can be induced at various steps in the above process flow, affecting significantly the BTBT transport. There are mainly two detrimental effects expected from such a situation: (i) interface-roughness scattering of carriers; (ii) charge trapping in quantum dots (QDs) formed by modulation of the thin silicon layers due to roughness.

Optimization of the nanoscale patterning is possible by refining EBL exposure parameters, resist development process and RIE etching process, as indicated in Fig. 1. Tests are necessary to be set up with systematic changes of the above parameters. Rigorous verification and validation via scanning electron microscopy (SEM), atomic force microscopy (AFM) or Kelvin probe force microscopy (KPFM) [20, 21] can

bolster control over patterning accuracy and surface smoothness.

3. Low-Temperature Electrical Characterization

Despite the challenges in the fabrication of *pn* tunnel diodes, there is valuable progress achieved in the past decade, which yielded valuable insights into BTBT transport in Si nanodevices. In this section, a typical device structure is first presented, corresponding to lateral *pn* diodes that we fabricated in silicon-on-insulator (SOI) substrates. Then, the behavior of one device exhibiting the tunnel-diode characteristics is shown as a representative example. Higher yields and enhanced functionality can be obtained once optimization of device fabrication and a deeper understanding of the physics become possible.

3.1 Lateral pn Tunnel Diodes in Silicon-on-Insulator Films

The devices discussed in this work are fabricated in SOI substrates, using CMOS-compatible technologies in a cleanroom environment. The top Si layer is first thinned down by sacrificial oxidation steps, followed by patterning of the large Si pads for leads and central area. Doping is first done with P-donors and then with B-acceptors, with different masks, as illustrated in Fig. 2(a), i.e., a ∼20-30-nm-thick Si_3N_4 mask against B-doping and, respectively, a ∼10-20-nm-thick SiO_2 mask against P-doping. In both cases, a protective ∼1-nm-thick SiO_2 layer is thermally grown before spin coating of the doping source.

The nanostructure patterning is done next, following a high-resolution EBL process, before passivation by thermally growing a thin layer of SiO_2 (a thicker SiO_2 layer, around 10∼20 nm, is usually deposited on top of this layer by an electron cyclotron resonance (ECR) technique). The nanowire is shown by two SEM images in Fig. 2(b). The final step consists in the formation of the Al electrodes with ohmic contacts on the p^+ and n^+ Si pads. More details about the fabrication processes are provided elsewhere [18, 19, 22].

3.2 Phonon-Assisted Band-to-Band Tunneling Transport

Even when dimensions are reduced gradually down to 10-100 nm, phonon-assisted tunneling still remains critical because the indirect-bandgap nature of Si is not expected to change [18]. As in the bulk (large-scale) devices, phonons are still needed to mediate BTBT transport in order to conserve the momentum in the interaction between conduction-band electrons and valence-band holes. If the devices are relatively large, we often observe current kinks close to the values corresponding to transverse acoustic (TA) and transverse optical (TO) phonons. An example is given in Fig. 3, for a lateral SOI pn diode with a thickness of approximately 10 nm and high doping concentrations, $N_D \approx 2.7 \times 10^{20} cm^{-3}$ and $N_A \approx 0.9 \times 10^{20} cm^{-3}$ (as estimated by a four-point probe technique on reference samples). The low-temperature (T = 5.5 K) Ip-Vp characteristics exhibit current humps and a first derivative (displayed on the right axis) reveals more clearly that these are consistent with contributions from TA and TO phonons in BTBT transport.

When the dimensions are reduced to form quasi-2D films (thickness of 5-10 nm), 2D quantization starts to emerge, leading to a spectrum of discrete energy states in

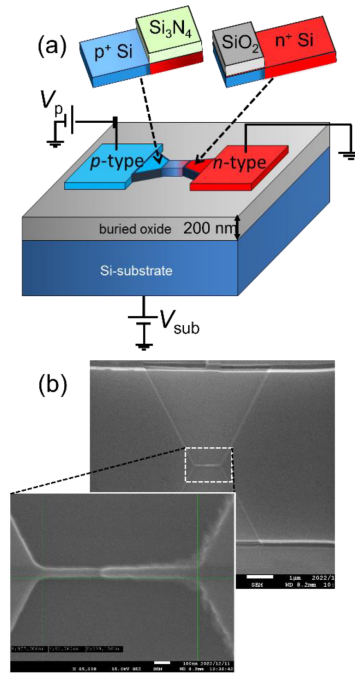

Figure 2. (a) Schematic device structure and doping masks (top) for a silicon-on-insulator (SOI) lateral *pn* diode. (b) SEM images of the central region of the device, with the zoom-in image showing the nanowire doped with B-acceptors on the left (*p*-type) and, respectively, with P-donors on the right (*n*-type).

the emitter and collector parts of the pn diode. The combination of these states with phonons has been shown to explain fairly well the set of fine features embedded in the forward- and reverse-bias regime [18]. However, further study is needed to clarify the practical implications of these findings.

In nanowire devices, the strong 1D quantization, combined with phonons, could allow the exploration of new functionalities at fundamental scales, even at atomic level, if dopant-atoms are taken into account.

3.3 Phonon-Assisted Band-to-Band Tunneling Transport

In tunnel diodes, gap states are known to be a limiting factor for the observation of high peak-to-valley ratios of the NDC peaks [3, 4, 5, 8]. This is because excess current can flow through these gap states, even when forward bias is applied in such a way that the direct BTBT current is forbidden. When tunnel diodes are strongly downscaled, the excess current may be governed by just one or a few gap states.

These gap states can be assigned to defects such as dislocations, interface traps or band tails, but a highly likely origin is clusters due to either donors or acceptors, remaining after compensation has also been taken into account. Such clusters can play the role of quantum dots (QDs), although the situation is quite different from that of single-electron tunneling in Si highly-doped nanoscale transistors [23, 24, 25]. In

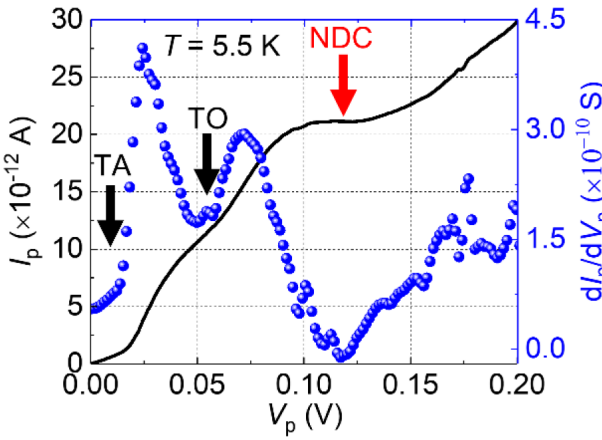

Figure 3. Electrical characteristics ($I_p - V_p$) at low temperature ($T = 5.5K$) in forward-bias regime for one SOI *pn* diode that exhibits the typical signatures of Esaki diodes: an NDC peak (marked by a red arrow) and current humps that can be ascribed to phonons by a first derivative (shown on the right axis). Phonons that can be identified with stronger signatures are transverse acoustic (TA) and transverse optical (TO) phonons (marked by black arrows).

the case of QDs formed in the depletion layer of a diode, there is a large asymmetry between the barriers on the two sides due to the large electric field naturally present in the depletion layer [19]. Even under such conditions, we previously reported single-charge tunneling working by the BTBT mechanism [19,22]. This can open new pathways for applying the BTBT mechanism to single-charge sensors, photodetectors or tunnel FETs.

3.4 Depletion Layers as Codoped Systems of Study

In nanoscale tunnel diodes fabricated in SOI films, the depletion layer is practically a codoped nanostructure. Codoped nanoscale systems are worth exploring even simply for the sake of the physics involved in such a material [22]. Codoping at high concentrations in thin (and ultrathin) Si layers may lead to the development of clusters or domains that are either *n*-type or *p*-type, alternatively. This can have a strong impact on the transport properties of Si, potentially transitioning its nature from that of a regular semiconductor towards that of a semimetal or a metal. It is also advantageous to have the ability to change the electric field with the biases, to apply gate voltages and to change temperature. All these practical capabilities can provide information about the heavily-doped compensated semiconductors (HDCS) [11], which can then be used to understand more deeply the critical physics behind the metal-insulator (Mott) transition in low-dimensional codoped systems.

Further studies are necessary to understand, design and fabricate devices with higher yields and enhanced functionality. For such purpose, it will be necessary to include also first-principles simulations in treating the atomic-level interactions between donors and acceptors, as recently started for codoped nanowire transistors [26]. Such insights can provide guidelines for the fabrication, interpretation and

physics that may emerge in atomic-level *pn* diodes.

4. Summary and Conclusion

This work illustrated the complex challenges in the fabrication of pn silicon-on-insulator tunnel diodes, but also the capabilities that can be leveraged for future electronics. The presentation of several key critical issues in fabrication can help trigger further optimization by introducing new and innovative ideas. At the same time, significant progress has been already made in demonstrating basic operation of nanoscale tunnel diodes by the BTBT mechanism. Among the phenomena revealed by the low-temperature electrical characterization of SOI lateral tunnel diodes, phonon-assisted BTBT was shown by an example to illustrate the possibility of using such downscaled devices to explore fundamental physics.

These results highlight the impact that codoped depletion layers of nanoscale tunnel diodes can have on band-to-band tunneling transport, a mechanism that promises to contribute more to alternative device designs in the next generations of electronics. Applications can be envisaged towards the development of nanowire tunnel diodes and tunnel field-effect transistors, but also towards photon and charge detection in the nanoscale depletion layer.

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