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RESEARCH ARTICLE

Control Scheme of Fast Charging System for Electric Motorcycles Using Phase-Shifted Full-Bridge Converter with Synchronous Rectification

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Abstract

This paper presents simulation of a fast-charging system for electric motorcycles using a Phase-Shifted Full-Bridge (PSFB) converter with synchronous rectification. The study compares two charging control strategies: the conventional mode-switching method and the proposed cascaded CC-CV control scheme. Simulation results show that while both methods effectively charge the battery, the proposed cascaded CC-CV approach provides smoother phase-shift transitions and reduces switching stress, especially during the constant voltage (CV) phase. Furthermore, the proposed method is able to maintain the stability of the transformer primary voltage, making it more likely to achieve Zero Voltage Switching (ZVS), which leads to higher efficiency and improved system reliability. These findings highlight the superiority of the proposed cascaded CC-CV control method in reducing power loss and enhancing converter performance for fast-charging applications for electric motorcycles.

Keywords: Charging Scheme, Electric Motorcycle, Fast Charging, Phase-Shifted Full-Bridge (PSFB), Synchronous Rectification (SR), Zero Voltage Switching (ZVS)

1. Introduction

The development of electromobility (e-mobility) is advancing as a solution to reduce carbon emissions and promote sustainable transportation. By utilizing electric power instead of conventional fossil fuels, e-mobility addresses environmental degradation and long-term energy sustainability. Electric vehicles (EVs), including electric motorcycles, play a central role in this transition as they offer a cleaner alternative compared

to internal combustion engine vehicles. Since EVs are becoming integral part of daily transportation, their development becomes more important. Studies shows that a 1% increase in EV sales in a city can lead to a 0.096% reduction in local CO_2 emissions and a 0.087% reduction in neighboring cities [1]. This indicates that widespread adoption of EVs not only improves air quality in urban areas but also provides environmental benefits to surrounding regions.

Despite the growing popularity of EVs, one of the major challenges to their broader adoption is the longer charging time required compared to the quick refueling as in internal combustion engine vehicles. The extended charging time required is often viewed as impractical, especially for users who are concerned about the convenience and availability of charging infrastructure [2], [3]. Some consumers are hesitant about adopting EVs due to concerns about the reliability of emerging technologies and the limited driving range per charge, which makes the transition from fossil-fueled vehicles to electric alternatives more difficult [4].

Modern EVs are usually equipped with automatic charging protocols that facilitate realtime parameter detection. These systems typically utilize communication standards such as SAE J2847/2836/2931/2953, IEEE 2030.5, and ISO 15118 [5], [6]. By adopting these standards, EVs and charging stations can exchange information to use the correct charging parameter, such as battery voltage, battery's state of charge (SOC), and current flow required. This interaction will protects battery health by preventing overcharging and overheating.

However, traditional electric motorcycles often lack these advanced charging protocols. Without these capabilities, chargers are unable to detect the proper voltage and current needed to safely charge the battery. Fast EV chargers must be designed to handle a wide range of voltage variations to ensure efficient power delivery across different battery configurations [7]. For traditional electric motorcycles, this voltage flexibility is essential to enable chargers to adapt to varying battery needs, ensuring fast and safe charging without undercharging or overloading the battery. As a result, the charging control algorithm must be capable of autonomously adjusting the current delivery based on changes in battery voltage, compensating for the lack of communication between the charger and the battery [8].

EV chargers use DC-DC converters to regulate voltage levels during the charging process. These converters may be classified as either isolated or non-isolated, with isolated converters generally being more suitable for EV applications. According to IEC 61851-25, isolation is a requirement for the DC EV supply equipment because the secondary circuit must be protected from the primary circuit by electrical separation [9]. Galvanic isolation mitigates electric shock risk and shields low-voltage control systems from high-voltage faults. In addition to safety, isolation also improves system performance, enhancing efficiency and power density, with typical power conversion efficiencies exceeding 92% and power ratings up to 10 kW for lowpower electric vehicles [10], [11]. Isolated topologies are often modified to support Zero Voltage Switching (ZVS), which reduces switching losses and improves converter efficiency.

As reviewed in [10], [12], [13], high-performance DC-DC converter topologies for EV applications are generally categorized into three types: Resonant Converters, Dual-Active Bridge Converters (DAB), and Phase-Shifted Full-Bridge Converters

(PSFB). These are all derivatives of modified half- or full-bridge converters. Resonant converters, such as LLC or CLLC topologies [14], [15], [16], achieve peak efficiencies between 96% and 98%, but their reliance on precise component values, precise resonance tuning, and complex design all contribute to increased in implementation costs.

DAB converters offer high efficiency, power density, and bidirectionality feature [17], [18]. However, bidirectionality is typically unnecessary for low-voltage and low capacity battery systems, such as those found in electric motorcycles. Moreover, recurring Vehicle-toGrid (V2G) operations can accelerate battery degradation [19]. In contrast, PSFB converters offer a simpler topology with modularity and easier control using phase-shift pulse-width modulation (PWM) to achieve ZVS. PSFB converters have demonstrated efficiencies of 95% to 98% and power densities exceeding 3 kW [20], [21], [22], [23], making them ideal for modular fast-charging applications in electric motorcycles.

Although many research on EV chargers have been conducted, few studies discuss electric motorcycles charger, especially on simpler models. Given the lower power requirement of these electric motorcycles, PSFB converters emerge as promising candidates for their charging systems. Conventional PSFB charging control algorithms typically rely on a mode-switching controller between current and voltage regulation [24], [25]. However, this method can introduce more dv/dt in the transformer primary because of the abrupt phase-shift changes during the switch to voltage control mode. This study proposes a cascaded control scheme using a voltage-limited current reference to regulate the charging process more smoothly, thereby reducing dv/dt on the transformer primary and switching stress.

2. System Design

2.1 General Concept

The proposed fast charger consists of six components: an AC-DC rectifier, a full-bridge switch, a step-down transformer, a fast-switching output rectifier, an LC filter, and a controller. Figure 1 illustrates the block diagram of the proposed charger. The AC-DC rectifier converts alternating current (AC) from the grid (220 - 240 V at 50 Hz or 110 - 127 V at 60 Hz) into high-voltage direct current (DC). his high-voltage DC is then fed to the full-bridge DC power switch to generate a square wave signal to the transformer's primary side. A controller generates PWM signals for four switches: the left half-bridge receives the regular PWM signal, while the right half-bridge receives the phase-shifted PWM signal relative to the left half-bridge PWM signal. Square-wave voltage is then stepped down by the transformer and delivered to the secondary side. The secondary side output is then rectified using full-wave bridge rectifier or synchronous rectifier (SR). SR is usually preferred over conventional diodebased rectifiers due to its superior efficiency under high-current operation.

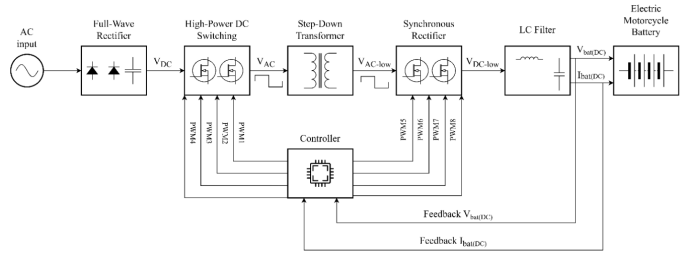

Figure 1. PSFB Fast Charger Block Diagram

The total power loss of a diode-based rectifier is determined by the conduction loss and reverse-recovery loss:

$$P_{loss(FWBR)} = P_{conduction(diode)} + P_{reverse} \tag{1}$$

The conduction loss is determined by the forward-voltage drop (V_F), the diode current (A), and the duty ratio (D):

$$P_{conduction(diode)} = V_f.I_f.D \tag{2}$$

Meanwhile, the reverse-recovery loss is determined by the reverse-recovery charge (Q_R), the reverse voltage ($V_{reverse}$), and the switching frequency (f)

$$P_{reverse} = Q_R.V_{reverse}.f_s \tag{3}$$

For synchronous rectification using MOSFETs, the total loss consists of conduction loss and switching loss:

$$P_{loss(SR)} = P_{conduction(MOSFET)} + P_{switching} \tag{4}$$

Conduction loss is expressed using the MOSFET on-state resistance ($R_{DS(on)}$):

$$P_{conduction(MOSFET)} = I_D^2.R_{ds(on)} \tag{5}$$

Switching loss depends on MOSFET drain-source voltage (V_{ds}), switching rise time (t_{rise}), switching falling time (t_{fall}), and switching frequency (f):

$$P_{switching} = \frac{1}{2}.V_{ds}.I_d.(t_{rise} + t_{fall}).f_s \tag{6}$$

Compared to the forward-voltage drop V_f of a diode, which typically ranges from 0.7 V to 1.5 V, the conduction loss in an SR configuration is significantly lower because the MOSFETs used in SR have very low on-state resistance $R_{DS(on)}$, typically in the milliohm range. This difference becomes increasingly significant at higher output currents, where the diode's fixed voltage drop produces losses that scale linearly with current. When ZVS is achieved, the switching losses $P_{switching}$ will be significantly reduced, leading to a notable improvement in the overall system efficiency.

The output voltage, which corresponds to the desired battery charging voltage, is then filtered by an LC filter. At higher power levels, larger filter components are generally required to effectively suppress output ripple. To reduce filter size, the switching frequency is typically increased above 100 kHz, as the ripple amplitude is inversely proportional to the switching frequency. This is made possible using high-speed devices like SiC MOSFETs.

Finally, the controller must be capable of driving eight switches top operate in both constant voltage (CV) and constant current (CC) modes. Feedback for the controller is received from voltage and current sensors. Voltage feedback is typically obtained via a resistor divider circuit, while current feedback is usually obtained by a shunt resistor or current transformer.

2.2 Topology

Figure 2 illustrates the schematic diagram of the proposed fast charger. With a properly sized input capacitor (C_{AC}), the AC-DC rectifier will produce DC link voltage equal to the peak value of the AC input signal. This DC link voltage is then applied to a full-bridge configuration, which generates a square wave voltage with a magnitude of $\pm V_{DC}$ on the primary side of the transformer. The PWM signals for S_1 and S_2 switches serve as reference signals, while S_3 and S_4 are phase-shifted PWM signals. The greater the phase shift, the higher the output voltage. The signal for S_2 is the complementary signal to S_1, and the signal for S_4 is the complementary signal to S_3. Both of these signals will have their own dead-time value. Selecting an appropriate dead time in a PSFB converter is crucial because it enables ZVS and prevents shoot-through. The full-bridge configuration is connected to a shim inductor L_S and a step-down transformer. This shim inductor must be selected based on the energy requirements for achieving ZVS, as this inductor helps dissipate the energy stored in the parasitic capacitances of the switches.

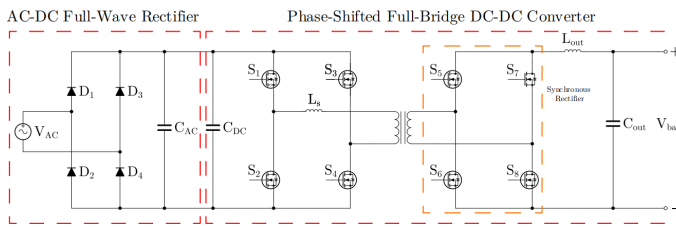

Figure 2. Proposed AC-DC electric motorcycle fast charger

The square wave voltage from the primary side induces a lower square wave voltage on the secondary side of the transformer. This secondary voltage is then rectified by SR in a fullbridge configuration. The SR follows the signals from S_1 and S_2, but can also be tuned independently for better efficiency under certain operating conditions. The output of the SR stage is then filtered using an LC filter to provide a clean, stable DC output for battery charging.

Because the AC-DC rectifier generates a stable DC-link voltage, system analysis can be simplified by focusing on the DC-DC conversion stage. Figure 3 shows

the equivalent circuit model of the DC-DC section. PSFB DC-DC converter will operates in five modes to regulate the output DC voltage, while achieving ZVS on the primary side. Figure 4 - Figure 8 illustrates the working principle of PSFB DC-DC converter with SR.

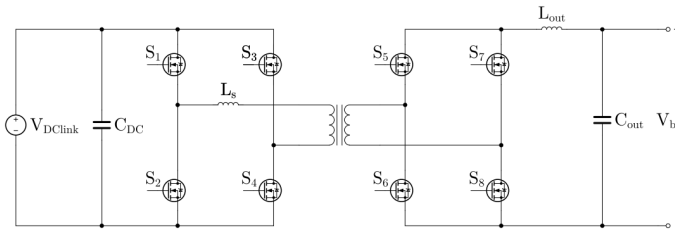

Figure 3. DC-link equivalent of proposed eletric motorcycle fast charger

1) Mode 1: S_1 ON, S_2 OFF, S_3 OFF, S_4 ON

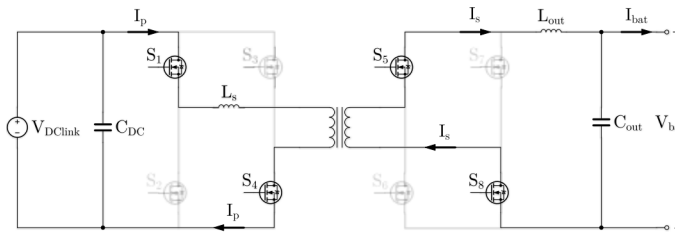

Figure 4. Mode 1 operation of PSFB converter

In Mode 1, switches S_1 and S_4 are turned on. This results in current flowing through the primary side of the transformer, transferring power to the secondary side.

2) Mode 2: S_1 ON, S_2 OFF, S_3 OFF, S_4 OFF

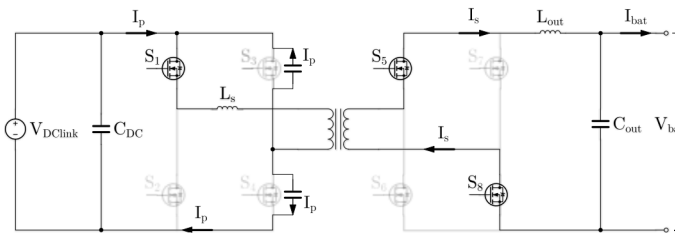

Figure 5. Mode 2 operation of PSFB converter

In Mode 2, only switch S_1 is turned on while the other switches remain off. In this mode, the primary current I_p continues to flow due to the parasitic capacitance of switch S_4, which gets charged to the value of the input voltage. Simultaneously,

the parasitic capacitance of switch S_3 discharges. Both of these events occur concurrently due to the energy stored in the resonant inductance. This phenomenon enables switch S_3 to turn on with ZVS, reducing switching losses.

3) Mode 3: S_1 ON, S_2 OFF, S_3 ON, S_4 OFF

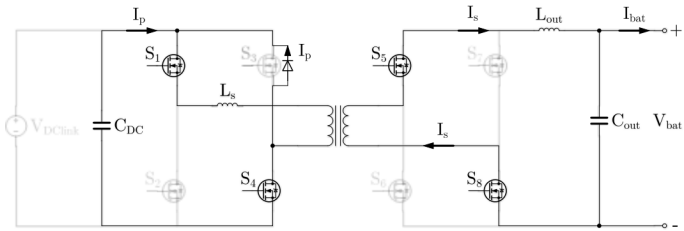

Figure 6. Mode 3 operation of psfb converter

In Mode 3, switches S_1 and S_3 are turned on. The primary current I_p flows through switch S_1 and the body diode of switch S_3. During this phase, switch $S3$ takes the current path, enabling the freewheeling phase, where the current continues to circulate without additional power transfer to the secondary side.

4) Mode 4: S_1 OFF, S_2 OFF, S_3 ON, S_4 OFF

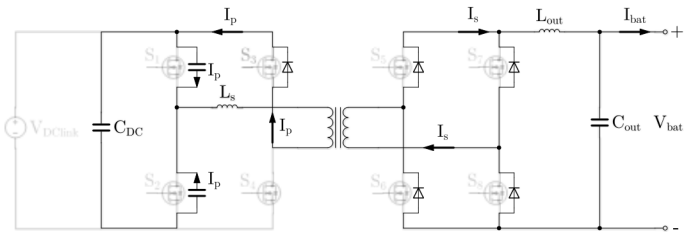

Figure 7. Mode 4 operation of PSFB converter

rent I_p flows through the output capacitance of S_1, which causes a decrease in the drain-tosource voltage. This transition allows switch S_2 to turn on with ZVS.

5) Mode 5: S_1 OFF, S_2 ON, S_3 ON, S_4 OFF

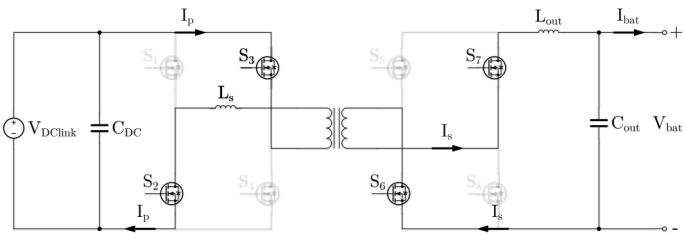

Figure 8. Mode 5 operation of PSFB converter

2.3 Synchronous Rectifier Special Case

To increase efficiency further, SR can be controlled under certain conditions. This control can be divided into three modes:

1) Mode 1 SR
   In Mode 1, which occurs under very low load conditions, the switches are turned off, resulting in classical diode rectification due to the body diodes of the switches. These switches are kept off because, at very low loads, the switching losses of the SR devices are higher when the switches are turned on.
2) Mode 2 SR
   In Mode 2, which operates under low to moderate loads, the SR switches are only turned on when the diagonal bridge signals from the full-bridge configuration overlap with the primary side signals. This timing ensures that the SR switches operate efficiently by minimizing unnecessary switching losses while still providing effective rectification. The overlap between primary and secondary signals helps synchronize the rectifiers with the voltage waveform of the primary side, reducing the likelihood of reverse recovery losses.
3) Mode 3 SR
   In Mode 3, where the converter operates under normal loads, the SR switches are turned on based on the signals from S_1 and S_2 in the full-bridge configuration. In this mode, the SR switches remain on for a longer period compared to Modes 1 and 2, as the current flow is.

2.4 Charger Output Regulation Algorithm

There are two methods for achieving CC and CV charging, such as traditional CC-CV method and multistage constant CC-CV method [8]. This study focuses on implementing traditional CC-CV method with simple algorithms for fast charging. Figure 9 illustrates the charging profile characteristics in traditional CC-CV mode. In this figure, it is shown that during charging, the charger must initially provide high current (CC) at lower voltage then lower its current value as the battery voltage rises and reaches a certain level. The charging current gradually drops until it reaches a very low value, signaling the battery is nearing full charge.

To achieve traditional constant current (CC) and constant voltage (CV) charging, the control algorithm must coordinate the current and voltage controller. Typically, two controllers are used: the current controller and the voltage controller. The current controller regulates the amount of current supplied to the battery, while the voltage controller adjusts the current supplied as the battery voltage approaches its maximum capacity. Both controllers are implemented using Proportional-Integral (PI) controllers.

For practical implementation on real hardware, such as in digital microcontrollers, the control laws must be expressed in discrete-time form. In this formulation, all control variables are evaluated at discrete sampling instants synchronized with the PWM switching period,

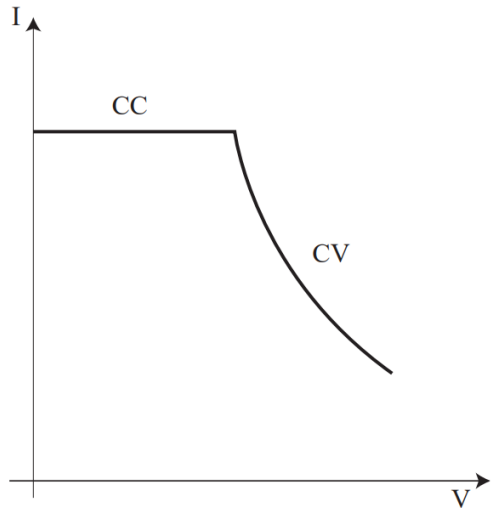

Figure 9. Charging profile graph in traditional CC-CV

$$t_k = kT_s,\ k = 0, 1, 2, \ldots$$

where T_s is the sampling period synchronized with the PSFB PWM.

This paper discusses two conventional methods for implementing CC-CV charging strategy for PSFB converter:

1) Method 1: Conventional Mode-Switching CC-CV Controller for PSFB
Figure 10 illustrates the conventional mode-switching method used in the CC-CV charging scheme. In this method, the CC and CV controllers operate independently. The phase output signal from the voltage controller is limited to the minimum and maximum battery voltage values. To determine which mode should be active, the controller continuously monitors the battery voltage. If the reference voltage V_{ref} is greater than the measured battery voltage V_{bat}, the charger operates in CC mode. Conversely, if V_{ref} is lower than V_{bat}, the charger switches to CV mode.
For current control loop, discrete-time current error is computed as:

$$e_{I(conv)}[k] = I_{set} - I_{bat(conv)}[k] \tag{7}$$

The integral term evolves to:

$$\chi_{I,CC(conv)}[k] = \chi_{I,CC(conv)}[k-1] + K_{i,CC(conv)} T_s e_{I(conv)}[k] \tag{8}$$

The unsaturated phase-shift command is:

$$\phi^*_{CC(conv)}[k] = K_{p,CC(conv)} e_{I(conv)}[k] + \chi_{I,CC(conv)}[k] \tag{9}$$

The actual phase-shift command applied to the converter is obtained by saturation:

$$\phi^*_{CC(conv)}[k] = sat(\phi^*_{CC(conv)}[k], \phi_{min(conv)}, \phi_{max(conv)}) \quad (10)$$

To prevent integrator windup, anti-windup is applied:

$$if\ \phi^*_{CC(conv)}[k] = \phi_{CC(conv)}[k],\ \ \chi_{I,CC(conv)}[k] = X_{I,CC(conv)}[k-1] \quad (11)$$

For voltage control loop, voltage error is defined as:

$$e_{v(conv)}[k] = V_{set} - V_{bat(conv)}[k] \quad (12)$$

The integral term updates as:

$$\chi_{I,CV(conv)}[k] = \chi_{I,CV(conv)}[k-1] + K_{i,CV(conv)} T_s e_{V(conv)}[k] \quad (13)$$

The unsaturated CV control output is:

$$\phi^*_{CV(conv)}[k] = K_{p,CV(conv)}[k] + \chi_{I,CV(conv)}[k] \quad (14)$$

With phase saturation yields:

$$\phi_{CV(conv)}[k] = K_{p,CV(conv)} e_{V(conv)}[k] + \chi_{I,CV(conv)}[k] \quad (15)$$

Anti-windup correction for voltage loop:

$$if\ \phi^*_{CV(conv)}[k] \neq \phi_{CV(conv)}[k],\ \chi_{I,CV(conv)}[k] = \chi_{I,CV(conv)}[k-1] \quad (16)$$

At each sampling instant, digital controller selects one of the two controller outputs:

$$\phi_{cmd}[k] = \begin{cases} \phi_{cc(conv)}[k] & \text{if } V_{bat}[k] < V_{ref} \\ \phi_{VC(conv)}[k] & \text{if } V_{bat}[k] \geq V_{ref} \end{cases} \quad (17)$$

This switching mechanism allows the system to transition between CC and CV during charging. However, this method introduces a potential drawback, where the phase output may spike rapidly from a low to high value in a short period. This sudden shift can cause additional stress on the switches because of the higher dv/dt, leading to higher switching losses. Another drawback is that the voltage-saturation block must be precisely calibrated to ensure the phase-shift controls signal accurately corresponds to the desired output voltage. Any miscalibration could allow the charging voltage response to exceed the battery's maximum safe limit.

2) Method 2: Proposed CC-CV Cascaded Controller for PSFB

and CV controllers operate dependently. The voltage controller generates a current reference, which is limited between zero and the maximum charging current setpoint ($I_{set(max)}$). The current reference (I_{set}) is then limited by the voltage controller output (I_{limit}). If the current setpoint is lower than the reference from the voltage controller, the current reference will be the same value as current setpoint.

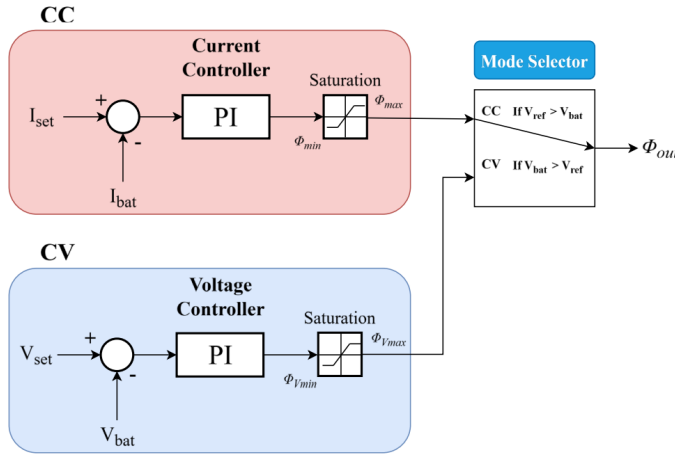

Figure 10. Conventional mode-switching method CC-CV controller for PSFB

This current reference is then used to regulate the output current based on the measured battery current. The output of the current controller is limited within a defined phase-shift range, which is typically calibrated between a minimum and maximum value to ensure the ZVS.
Outer voltage loop will generate current limit reference, where voltage error is defined as:

$$e_{V(cas)}[k] = V_{set} - V_{bat(cas)}[k] \tag{18}$$

Voltage-loop integrator update is:

$$\chi_{I,V(cas)}[k] = \chi_{I,V(cas)}[k-1] + K_{i,V(cas)} T_s e_{V(cas)}[k] \tag{19}$$

Unsaturated current limit reference is defined as:

$$I^*_{limit} = K_{p,V(cas)} e_{V(cas)}[k] + \chi_{I,V(cas)}[k] \tag{20}$$

Current limit is saturated to the allowable charging range:

$$I_{limit} = sat(I^*_{limit}, 0, I_{set,max}) \tag{21}$$

Anti-windup applies when:

$$if\ I^*_{limit}[k] \neq I_{limit}[k],\ \chi_{I,V(cas)}[k] = \chi_{I,V(cas)}[k-1] \tag{22}$$

The effective current reference used for inner-loop control is

$$I_{ref}[k] = min(I_{set}, I_{limit}[k]) \tag{23}$$

Current error is defined as:

$$e_{I(cas)}[k] = I_{ref}[k] - I_{bat(cas)}[k] \tag{24}$$

The current-loop integrator update is:

$$\chi_{I,I(cas)}[k] = \chi_{I,I(cas)}[k-1] + K_{i,I(cas)} T_s e_{I(cas)}[k] \tag{25}$$

The unsaturated phase-shift command is:

$$\phi^*_{cmd}[k] = K_{p,I(cas)} e_{I(cas)}[k] + \chi_{I,I(cas)}[k] \tag{26}$$

The applied phase shift command is obtained through saturation:

$$\phi_{cmd}[k] = sat(\phi^*_{cmd}[k], \phi_{min(cas)}, \phi_{max(cas)}) \tag{27}$$

Anti-windup is applied when:

$$if\ \phi^*_{cmd}[k] \neq \phi_{cmd}[k],\ \chi_{I,I(cas)}[k] = \chi_{I,I(cas)}[k-1] \tag{28}$$

This method offers two main advantages compared to the conventional mode-switching method. First, it enables a smoother transition of phase-shift, leading to lower *dv/dt*. Second, it allows the system to automatically limit the charging current based on the battery's capacity. For instance, if the set current is 50 A but the battery can only safely handle 20 A, the system will automatically restrict the output current to 20 A, protecting the battery from overcurrent conditions

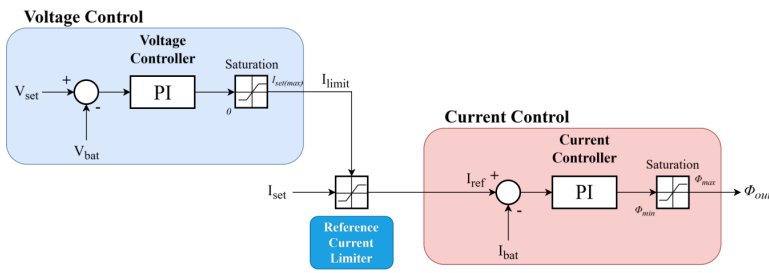

Figure 11. Proposed cascaded CC-CV controller for PSFB

3. Results and Simulation

In this study, simulations were conducted using PSIM circuit simulation to evaluate and compare the performance of these two charging control methods using discrete controller. The primary objective of the simulation was to analyze the characteristics of state-of-charge (SOC), battery voltage, charging current, and phase-shift control signals under the two distinct charging algorithms. Since the two controllers differ primarily only during the CV mode, the analysis will focus on this condition. Method 1 refers to the conventional mode-switching control approach, while Method 2 refers

to the proposed cascaded CC-CV control strategy. The system characteristics during CC mode will also be discussed. However, because both methods operates in the same condition on CC mode, no distinction between the two is observed in this operating region. It is important to note that all analyses presented in this section are based solely on simulation results and have not yet been experimentally validated.

3.1 Simulation Parameters

3.1.1 PSFB Charger Parameters

Table 1. PSFB charger simulation parameters

Parameters	Value
AC-link input voltage	230 V 50Hz
DC-link voltage (after rectifier)	325 V
Switching Frequency	100 kHz
Transformer ratio	$n_p : n_s$=2:1
Output voltage target	36 V - 112 V
Output current target	0 A - 50 A

3.1.2 Battery Parameters

Table 2. Battery simulation parameters

Parameters	Value
Number of cells	20
Cell nominal voltage	3.6 V
Cell max voltage	4.2 V
Rated voltage	72 V
Rated capacity	50 Ah
Rated energy	3.6 kWh
Maximum charge voltage	84 V

3.2 Results

3.2.1 Charging Characteristics

15 A constant-current charge. In the early charge phase (0 – 10 % SOC), the voltage increases significantly from approximately 56 V to 76 V. Between 10 % and 80 % SOC, the voltage rises slowly, increasing only from 76 V to 80 V, which indicates that the cells require progressively more energy per unit SOC as polarization and internal resistance effects become significant. Beyond 80 % SOC, the voltage curve exhibits a shallow upward curvature.

Figure 12(b) provides a detailed view of the battery voltage behavior when nearing full charge, within the 99 – 100 % SOC range. In this region, the voltage gradually increases from approximately 84.56 V to 84.75 V, slightly exceeding the specified maximum battery voltage. This observation suggests that the charger's CV regulation

may require adjustment to a higher setpoint to ensure complete charging without prematurely terminating the process. These results also indicate that the battery is capable of sustaining a 15 A charging current without experiencing excessive voltage rise under the conventional and proposed charging algorithm. Based on this analysis, the charging voltage setpoint is set at 84.7 V for all subsequent test conditions, as the CV characteristics and regulation behavior become prominent only within this narrow SOC range near full charge.

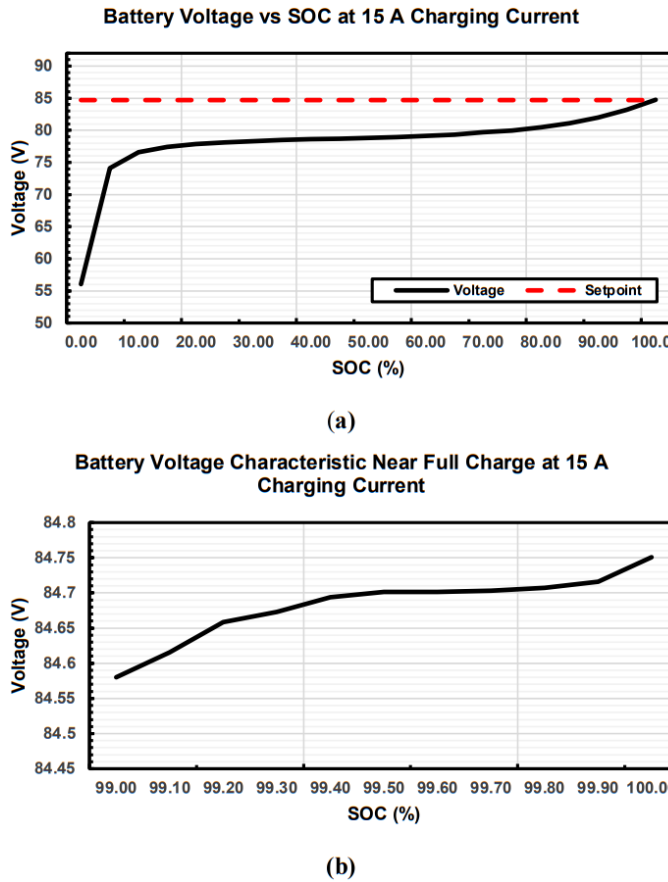

Figure 12. Battery voltage at different SOC percentage: (a) From 0 % to 100 %, (b) Close up from 99% to 100%

setpoint. PSFB converter initially delivers a steady 15 A before reaching CV region. As the battery reaches CV region, the current starts to drop off at above 99.5 % SOC. The current taper sharply until it nearly reaches zero when the battery is fully charged. This results shows that the PSFB topology can regulate current and voltage reliably and terminate charging when the battery is fully charged, making it well suited for electric motorcycle fast charger applications.

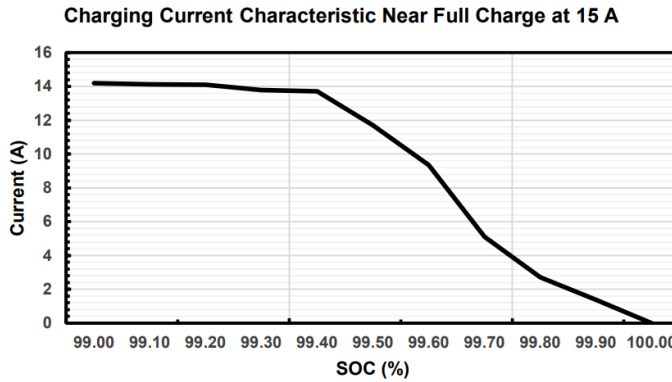

Figure 13. Charging Current Characteristic Near Full Charge at 15 A

3.2.2 CC Mode

Figure 14 illustrates the dynamic response of the proposed PSFB SR charger when the current setpoint is stepped from 0 A to 15 A at t = 1 ms. Figure 14(a) illustrates the charger's response to the change. At t < 1 ms, the output current negative due to the lack of current setpoint. This is a common behavior during startup in simulation environments for battery charging simulation, where the current flows from the battery to the converter. At zero setpoint, the output voltage of the charger is much lower than the battery. Because of capacitive and inductive effects on PSFB, the battery discharge to reverse the current flow and store energy on these components so the voltage comes back down. However, in real hardware, usually this behavior only produces very small current in the order of mA. The controller brings the current to within 5% of the setpoint in under 2 ms, demonstrating quick response even when the system dynamics are fluctuating.

Figure 14(b) presents a close-up of the steady-state current ripple after the step response. Even after settling, the battery current exhibits a sinusoidal oscillation with a value approximately 13.5 ± 1.5 A around the 15 A target. This ripple arises from the PSFB's highfrequency switching and the finite bandwidth of the inner current loop. PI controller only corrects low-frequency deviations, therefore it is unable to counteract the fast switchingfrequency harmonics. As a result, when the graph is zoomed out, the output charging current appears to have an offset, which is, in fact, a sinusoidal oscillation. This is evident from the current peaks reaching the setpoint yet failing to fully stabilize the converter due to limitation of bandwidth. This is acceptable as long as the ripple current occurs over a very short period of time and the average current remains tightly regulated around the charging current setpoint. In real hardware, we can compensate this by choosing very large output capacitor to have a very stable output voltage and current.

Figure 14(c) shows the corresponding phase-shift control signal. At the start of step value, the controller saturates the phase shift to its maximum value. Then, the phase control signal drops significantly and settles at approximately 75°, the value required to sustain 15 A in steady state. When the setpoint changes from 0 to 15

A, the PI controller error becomes very high, causing it to increase the phase duty cycle to compensate for the sudden change. This phenomenon results in the converter having a sudden high phase duty cycle. To address this, methods such as feedforward control, soft-start ramps, or lowering the PI gain can be used. However, these results confirm that in CC mode, the converter can achieve a quick and precise transient response with a simple PI controller.

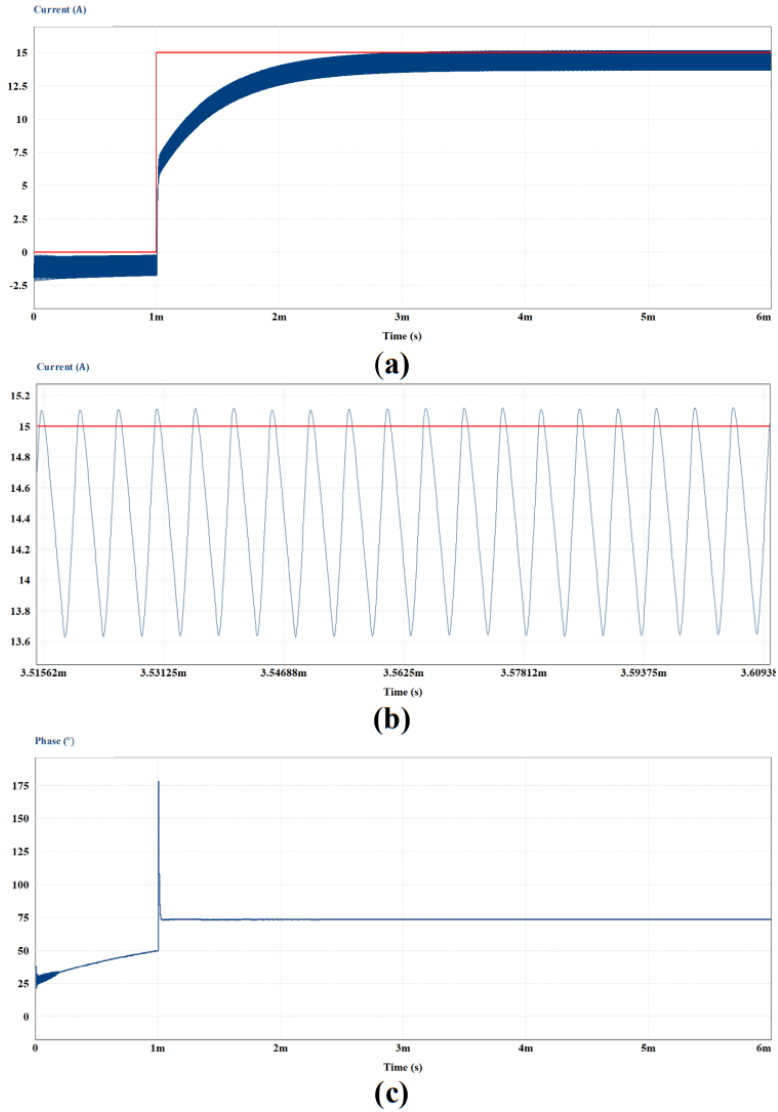

Figure 14. Transient response of the proposed charger at 15 A charging setpoint: (a) Output current, (b) Close-up of the steady-state current ripple, (c) Phase-shift value

3.2.3 CV Mode Transition

In CV mode transition, the two control methods behave differently. Figure 15 presents the phase-shift control signal responses as the battery voltage approaches the charging setpoint. In the first method, shown in Figure 15(a) and Figure 15(b), the phase-shift control signal changes rapidly as in a square wave signal. This happens because the voltage and current controllers operate independently, each controlling different phase-shift values, causing abrupt mode switch between the two control loops. On the other hand, the second method, as shown in Figure 15(c) and Figure 15(d), provides a much smoother transition. This result indicates that the proposed cascaded CC-CV control algorithm from the second method provides a significant improvement over the conventional mode-switching method, reducing *dv*/*dt* and stress on the switching devices.

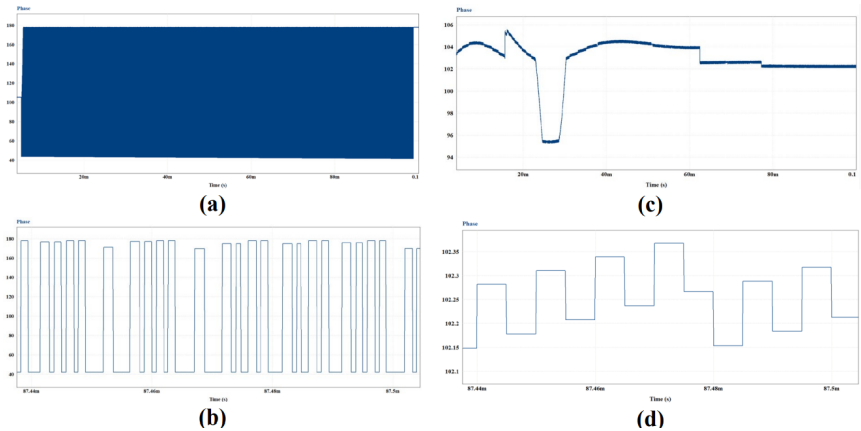

Figure 15. Phase-shift control signal at CV mode transition: (a) Conventional mode-switching, (b) Conventional mode-switching close-up, (c) Proposed cascaded CC-CV, (d) Proposed cascaded CC-CV close-up

The fluctuations in the phase-shift control signal directly affect the primary-side voltage waveform. In the conventional mode-switching method, as shown in Figure 16(a), switching between CC and CV modes creates an irregular primary voltage with erratic pulse width variations and frequent failures to reach the full DC-link amplitude. This lack of a true steadystate condition prevents consistent ZVS, increases *dv*/*dt*, increases stress on the semiconductor devices, and lowering overall efficiency. In contrast, Figure 16(b) demonstrates that the proposed cascaded CC-CV controller produces a steady, fixed-amplitude square wave under steady-state conditions. This stable waveform ensures reliable ZVS turn-on, reduces switching losses, and achieves superior performance compared to the conventional modeswitching approach.

Figure 17 shows the frequency-domain analysis of transformer primary voltage during CV transition using Fast Fourier Transform (FFT) feature in PSIM. Results demonstrate that the proposed cascaded CC-CV method reduces high-frequency *dv*/*dt* content in the primary voltage waveform by 20.89% within the 150 kHz to 30 MHz. This reduction in highfrequency components leads to lower EMI emissions and less electrical stress on the transformer windings.

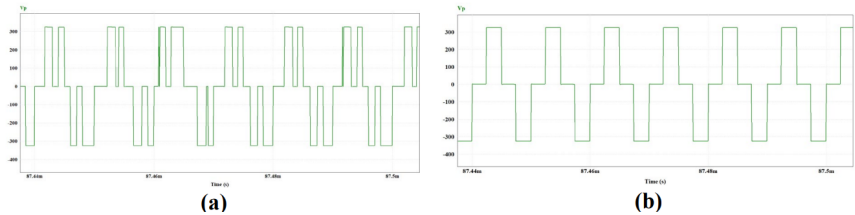

Figure 16. Transformer primary voltage at CV mode transition: (a) Conventional mode-switching, (b) Proposed cascaded CC-CV

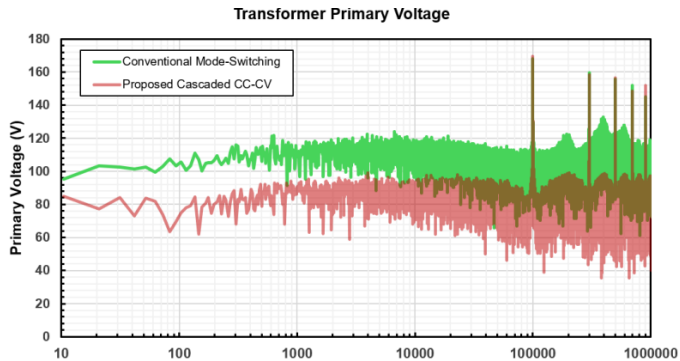

Figure 17. Frequency-domain analysis of transformer primary voltage

Figure 18 compares the charging characteristics during the transition phase for both control methods. In the conventional mode-switching method (Figure 18(a) and Figure 18(b)), the battery voltage stabilizes around the charging setpoint, while the current rapidly decreases. In contrast, the proposed cascaded CC-CV method (Figure 18(c) and Figure 18(d)) shows a second-order response, where both the voltage and current initially overshoot the setpoint before gradually settling. This second-order behavior results from the cascaded control's feedback loops, which initially correct the error more aggressively before reaching the steady state condition.

As system reaches steady-state conditions, the phase-shift control signal in the cascaded method remains stable, whereas in the conventional mode-switching method, the phase-shift control signal continues to fluctuate. These fluctuations in the conventional mode-switching method cause irregularities in the voltage waveform, as evidenced in the primary voltage irregularities. While the conventional mode-switching method has a faster current drop response, the overall performance advantage is minimal. The real benefit of the cascaded CCCV method is its ability to maintain a stable primary voltage to achieve ZVS while still maintaining the ability to drop the charging current. These results demonstrate that the proposed cascaded CC-CV control method provides superior performance in CV mode transition.

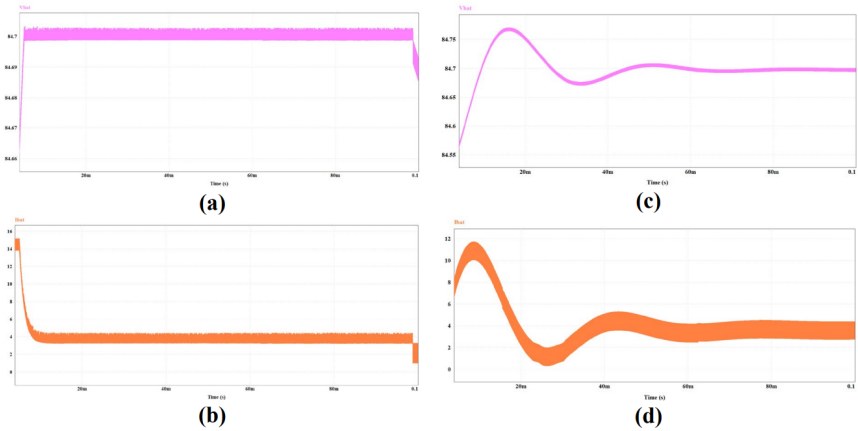

Figure 18. Charging characteristics at CV mode transition: (a) Battery voltage with conventional mode-switching (b) Charging current with conventional mode-switching (c) Battery voltage with proposed cascaded CC-CV (d) Charging current with Proposed cascaded CC-CV

3.2.4 CV Mode (Near Full-Charged)

At the end of the charging phase, the behaviors of the two control methods differ again. Figure 19 shows the phase-shift control signal as the battery nears full charge. Similar to the transition during CC-CV mode, the proposed cascaded CC-CV control method demonstrates better performance compared to the conventional mode-switching approach, with a smoother and more stable phase-shift control signal compared to the conventional method.

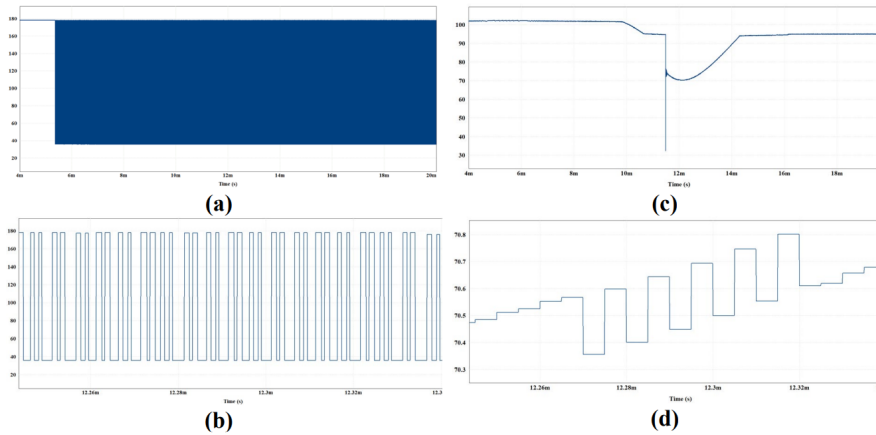

Figure 19. Phase-shift control signal when charging voltage is nearing charging setpoint: (a) Conventional modeswitching, (b) Conventional mode-switching close-up, (c) Proposed cascaded CC-CV, (d) Proposed cascaded CCCV close-up

In a similar manner to the transition phase, the rapid changes in the phase-shift control signal near full charge in the conventional mode-switching method lead to distortion of the transformer's primary voltage waveform, as shown in Figure 20. This distortion also introduces additional *dv*/*dt* and switching losses.

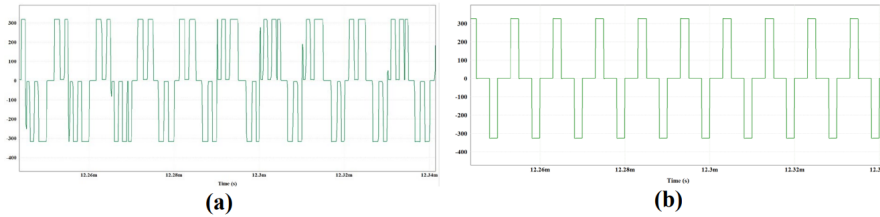

Figure 20. Transformer primary voltage at steady-state when charging voltage is nearing charging setpoint: (a) Conventional mode-switching, (b) Proposed cascaded CC-CV

Figure 21 compares the terminal behavior of the battery as it approaches full charge under the both control schemes. In the conventional mode-switching method (Figure 21(a) and Figure 21(b)), the battery voltage rises smoothly towards the setpoint and then oscillates around that value. However, this behavior is strongly influenced by the voltage controller, which introduces greater complexity due to the need for precise phase tuning. Meanwhile, the charging current decays gradually to zero, providing a predictable end-of-charge indicator. In contrast, the proposed cascaded CC-CV controller (Figure 21(c) and Figure 21(d)) produces a small voltage overshoot above the setpoint before it settles slightly below. This brief transient momentarily drives the current increases the current, which then spikes before returning to a steady level. Although this spike complicates end-of-charge detection, it has minimal impact on overall charging time and battery health. The controller must monitor whether the current oscillates slightly above and below zero to indicate end-of-charge.

The proposed cascaded CC-CV control scheme achieves smoother voltage settling and reduced phase-shift changes at the end of charge, resulting in lower device stress and higher overall efficiency. This advantage becomes even more significant when higher charging currents are allowed. At lower battery voltages and higher charging currents, the output voltage may oscillates around the target setpoint, allowing increased current flow while maintaining safe operating conditions. During longer charging periods, the impact of rapid phase-shift transitions on overall efficiency and device longevity becomes more significant. Therefore, despite the conventional mode-switching method offering simpler end-of-charge detection and smoother transition at the end of charge, the proposed cascaded CC-CV control demonstrates superior converter performance and efficiency, with only a minor increase in detection complexity.

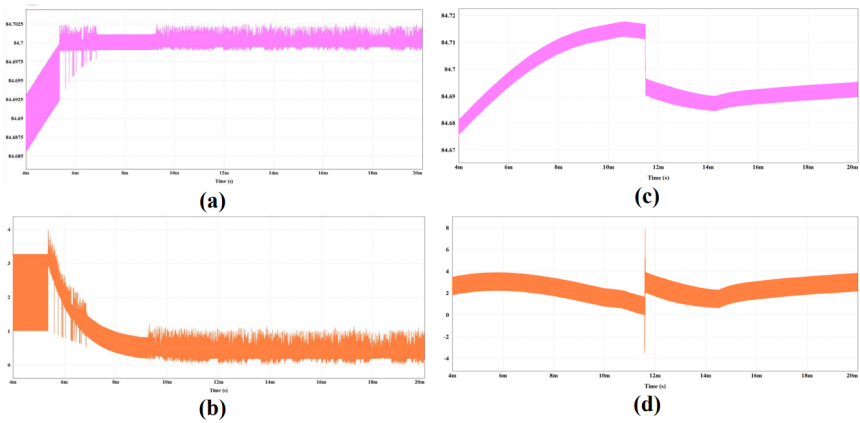

Figure 21. Charging characteristics when nearing full-charged: (a) Battery voltage with conventional modeswitching (b) Charging current with conventional mode-switching (c) Battery voltage with proposed cascaded CCCV (d) Charging current with Proposed cascaded CC-CV

4. Conclusion

In this paper, a proposed cascaded CC-CV control scheme were presented for PSFB converter. Simulation results show that, compared to the conventional mode-switching method, the proposed control strategy improves system performance by maintaining a more uniform transformer primary voltage and providing a more stable phase-shift control signal during both CV transition and end-of-charge phases. Frequency-domain analysis reveals a 20.89% reduction in high-frequency *dv/dt* during CV transition, which indicates lower EMI and reduced electrical stress on transformer windings. These improvements result in higher system efficiency, better EMI performance, and greater reliability, making the proposed method a promising solution to test on experimental results for future high-performance EV charger implementations.

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