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RESEARCH ARTICLE

A High Gain Concurrent Dual-band Low-Noise Amplifier in 130-nm BiCMOS Technology

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Abstract

This paper presents a fully integrated concurrent 15/30-GHz dual-band low-noise amplifier (LNA). The proposed concurrent LNA IC is designed and simulated in 130-nm BiCMOS technology. The new passive LC notch filter is proposed to realize high gain and low noise figure over dual-band frequency, simultaneously. The simulated BiCMOS LNA IC has exhibited peak gains of 30.1/23.7 dB at 15/30-GHz, respectively, with 20-mW power consumption from 1-V supply. The concurrent dual-band LNA achieves noise figure of 2.2/2.9-dB and IIP3 of -18.2/-8.8 dBm at the respective passbands. Therefore, the proposed dual band concurrent LNA IC is applicable to front-end RF receivers for Ku-Band and Ka-Band systems.

Keywords: Low Noise Amplifier, BiCMOS, Ku-Band, Ka-Band, LC notch filter

1. Introduction

In recent years, utilizing concurrent technique in receiver system has gained significant interest. Comparing to the multi-band receiver system developed from single band receiver, the concurrent multi-band technique has numerous advantages in terms of optimum size, cost, power consumption and ease for integration. For this reason, the research on concurrent multi-band low noise amplifier (CM-LNA) as the first block of receiver has improved significantly. This progress underscores the industry's shift towards more efficient, cost-effective solutions that do not compromise on performance. The development of CM-LNA technology has paved the way for more compact and energy-efficient receiver systems, enabling broader applications across various sectors. Innovations in this field are driving the future of communications technology, promising enhanced signal quality and reliability. As this technology continues to evolve, it holds the potential to revolutionize the way we design and utilize

communication devices, making them more adaptable to the increasing demands for multi-band capabilities. The continuous improvement in CM-LNA research highlights its critical role in achieving superior receiver performance while adhering to the pressing requirements for efficiency and integration in modern electronic systems.

Several CM-LNAs have been reported in recent studies [1-4], highlighting various approaches to enhancing performance. For instance, an active notch filter introduced in [1] aims to achieve stop-band rejection for dual-band applications, a technique that effectively mitigates the resistive losses associated with the load inductor. Yet, this solution leads to increased power dissipation due to the inclusion of extra active components. Another study [2] leverages positive feedback to achieve desired input/output matching at specific frequencies, however, this method necessitates a three-stage circuit design, significantly enlarging the circuit's footprint and escalating costs. A novel active notch filter suggested in [3] to compensate the low Q-factor of inductors, but it contributes to greater power consumption of the LNA due to the addition of an extra transistor. These studies underscore the ongoing quest for optimizing CM-LNA designs, balancing between performance improvements and the practical limitations of power efficiency and circuit complexity.

In this paper, we present a concurrent dual-band low noise amplifier for 15/30-GHz applications in 0.13-μm SiGe BiCMOS technology. A new load impedance is proposed to achieve a high and balance gain over multiple frequency. In addition, the proposed input matching circuits without series inductor reduce the area and eliminate the noise contribution of the gate inductor. The novel concurrent dual-band LNA achieves high gain and excellent noise figure performances.

2. Proposed Concurrent Dual-Band Low Noise Amplifier

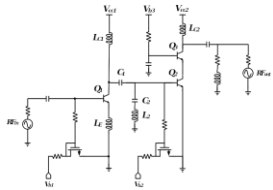

Figure 1. Proposed concurrent dual-band LNA

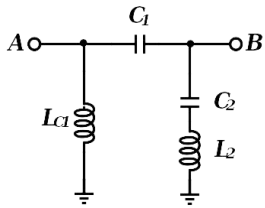

Figure 2. Proposed load inductor configuration

The schematic circuit of proposed dual-band concurrent LNA is illustrated in Figure 1. It is consisted of two-stage circuits; current-emitter transistor with source inductive degeneration for the first stage and cascode transistor configuration for the second stage. The dual-band characteristic is achieved using proposed load inductor shown in Figure 2. Since the wideband response covering both desired frequency is required, a low-Q inductor is chosen for LC1 with a center frequency of 22.5 GHz. The series L2-C2 determines the location of notch frequency. Therefore, a high Q-factor of L2 is very important to obtain sharp filtering. The inter-stage matching between 1st stage and 2nd stage of LNA is handled by the proposed load inductor and drain capacitance of Q_1, simultaneously, without any additional matching components hence minimize the die area of LNA.

Moreover, the proposed load inductor plays a dual role in effectively managing the inter-stage matching between the LNA's first and second stages. This is accomplished in concert with the drain capacitance of transistor Q_1, obviating the need for separate matching components. Such a design innovation not only streamlines the signal processing pathway but also significantly conserves die area, an attribute of paramount importance in the miniaturization of modern electronic devices. Additionally, this approach imbues the LNA with greater flexibility and compatibility in a broader range of applications, by facilitating easier integration into complex systems without the burden of increased size or complexity. The strategic incorporation of these design elements not only elevates the performance metrics of the LNA but also enhances its economic and practical viability, setting a new benchmark for dual-band LNA design.

The input matching and output matching circuit of the proposed LNA is optimized to cover the wideband operation of 15 to 30 GHz. The gate inductor is not employed to provide lower noise figure for large Q_1. Although the gate inductor provides a better noise match, the noise contribution of gate inductor is significant in large transistor design. Therefore, in the proposed circuits the optimum source reflection coefficient, opt, is only provided by L_E and C_{gs}. In order to minimize the effective-transconductance degradation, the transmission line is employed as source inductive degeneration L_E and carefully selected for stability, gain matching and noise matching, simultaneously. The EM simulations are performed to verify the layout geometry of the circuits, especially for inductors and component interconnections.

Figure 3 shows the simulation procedures to determine an operating point of Q_1. Since Q_1 is the first active device of the circuits, the collector current density (Jc) is chosen to get optimal NF and Gain. As shown in the figure, by selecting Vbe of 0.845 V and Jc of 2.95 mA/μm2, a minimum NF and an optimum safe margin of Gmax is obtained simultaneously. The emitter length for Q_1 is chosen as 7.5 μm with 0.13 μm of emitter width to match the optimum noise source resistance of 50 ohm. For a double emitter device of Q_1, the collector current by this condition is 5.2 mA.

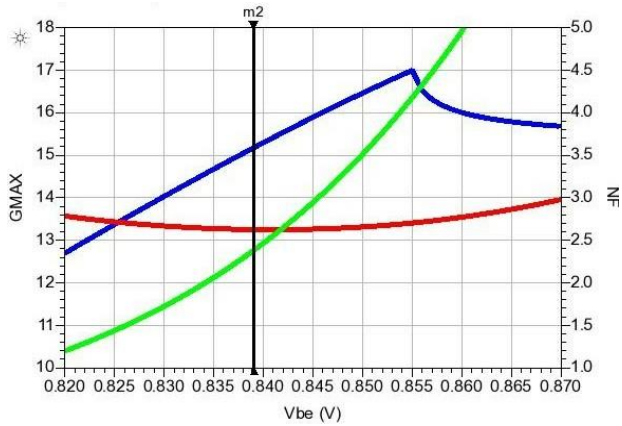

Figure 3. Vbe versus collector current density (Jc), Gmax and NF

In the design of the second stage, the careful biasing of transistors Q2 and Q3 is crucial for hitting the desired benchmarks of amplification and linearity, ensuring the LNA's performance meets specific requirements. The choice to use a similar device size for Q_1, Q_2 and Q_3 aids in simplifying the design process and maintaining consistency in performance across stages. This decision directly influences the operating conditions of the second stage, notably setting the collector current at 5 mA, a figure that reflects a balance between efficiency and output quality. Consequently, when considering the combined operation of both stages, the total power consumption is meticulously calculated to be 15.2 mW.

3. Simulation Results and Discussion

Figure 4 presents the simulated results for the input return loss (S11) and small signal gain (S21) of the proposed concurrent dual-band LNA, highlighting its performance over the frequencies of interest. Notably, the S11 values (depicted by the red line) remain below -12 dB for both targeted frequencies, indicating a highly effective impedance matching that minimizes reflection and maximizes energy transfer into the LNA. The blue line representing the simulated S21 shows that the proposed LNA achieves a commendable gain of more than 22 dB across bandwidths of 4 GHz and 9 GHz for frequencies of 14 GHz and 28 GHz, respectively. Furthermore, as illustrated in Fig. 4, the output return loss (S22) for the LNA is also maintained below -12 dB for both frequencies, ensuring efficient signal transmission from the LNA. These characteristics underscore the proposed LNA's capability to provide excellent input and output return losses, which are crucial for minimizing signal degradation and enhancing overall system performance over the specified frequency range.

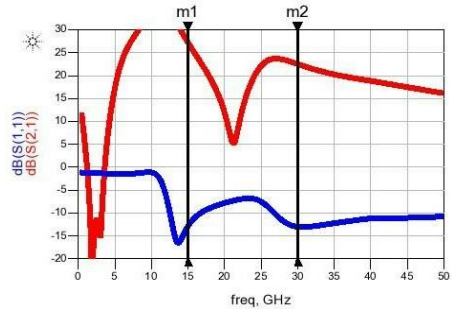

Figure 4. Simulated small signal S-parameter of proposed LNA at a supply voltage of 1 V

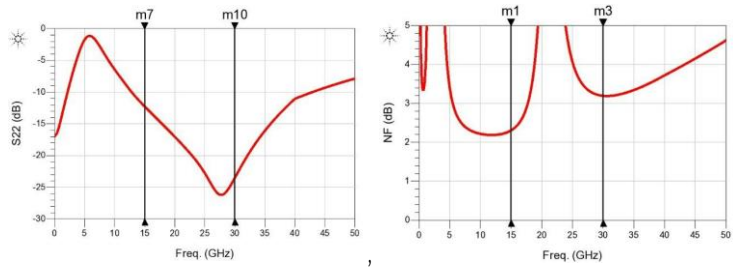

Figure 5. Simulated output return loss of proposed LNA at a supply voltage of 1 V

Figure 5 displays the simulation results for the noise figure (NF) performance of the proposed LNA design. It reveals that at frequencies of 15 GHz and 30 GHz, the simulated noise figures are measured at 2.4 dB and 3.2 dB, respectively, indicating favorable noise performance across the dual-band operation. Additionally, Figure 6 showcases the simulated stability factor (Kf) of the proposed LNA design across a wide frequency range. The stability factor, consistently exceeding 1 over the entire frequency spectrum, signifies the robustness and reliability of the circuit's operation, ensuring stable performance even under varying operating conditions. These simulation outcomes corroborate the efficacy of the proposed LNA design in delivering low noise performance and stable operation across the desired frequency bands, critical attributes for high-performance receiver systems in modern communication applications.

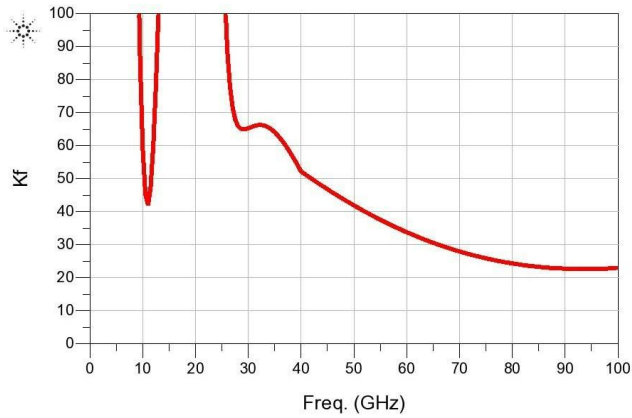

Figure 6. Simulated stability factor (Kf) of proposed LNA

Figure 7 exhibits the simulated noise figure versus drain current characteristics of the first stage of the proposed LNA design. The pink and red lines correspond to the noise figure performance across varying drain currents for frequencies of 15 GHz and 30 GHz, respectively. Notably, for both frequency bands of interest, the minimum noise figure is attained within the range of 5-7 mA of drain current. This finding underscores the importance of optimizing the operating conditions, particularly the drain current, to achieve optimal noise performance at the desired frequencies. By identifying the drain current range that yields the lowest noise figure, designers can effectively tailor the LNA's operation to meet specific performance objectives, ensuring superior signal reception and processing capabilities across the dual-band spectrum.

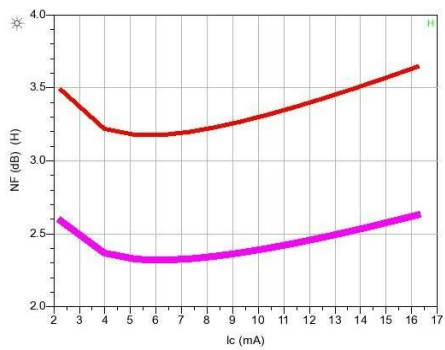

Figure 7. Simulated Noise Figure (NF) versus drain current (IC) of proposed LNA

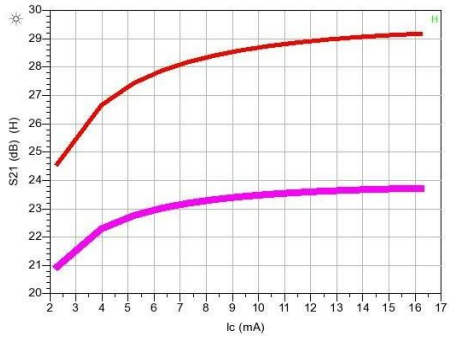

Figure 8. Simulated small signal gain (S21) versus drain current (IC) of proposed LNA

Figure 8 illustrated the simulated small signal gain (S21) of the proposed circuits versus drain currents. The pink line and red line represent the small signal gain performance over drain current variations for 15 GHz and 30 GHz, respectively. Since the target of small signal gain over both frequency of interest is better than 20 dB, the small drain current of 1st stage is enough to fit it. The gain will be saturated when the drain current of 1st stage is around 5-6 mA as depicted in Figure Figure 8. Therefore, comparing two performance of noise figure and small signal gain over 1st stage drain current, the 5.2 mA of drain current is selected to provide best performance of noise figure and gain over than 20 dB.

The simulated IIP3 versus 2nd stage drain voltage at stable drain current of 6.7 mA is shown in Figure 9. The required of 2nd stage drain current for achieving the power consumption target of 15 mW is determined to be 6.7 mA. Therefore, the optimum drain voltage for cascade stage in 2nd stage of proposed circuits is required to obtain good linearity performance. As shown in Fig. 9, the optimum 2nd stage drain voltage in the proposed concurrent dual band LNA to get best performance of IIP3 at 30 GHz is 1.5 V.

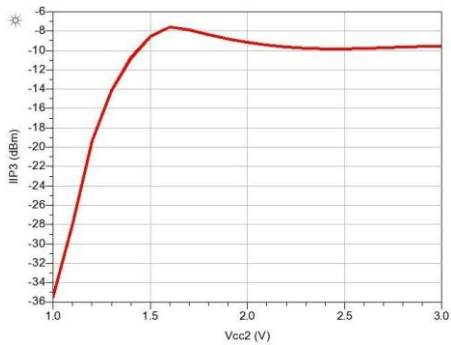

Figure 9. Simulated IIP3 versus drain voltage (VCC2) of 2nd stage of proposed LNA with constant drain current of 6.7 mA

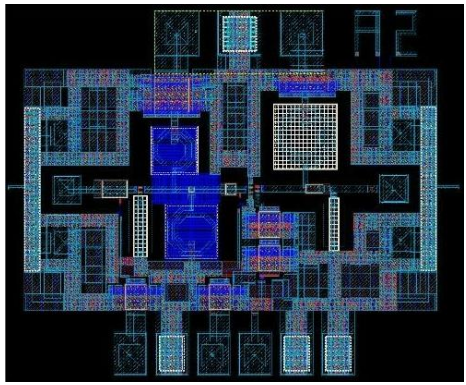

Figure 10. Layout design of proposed LNA

Figure 10 shows the layout design of proposed LNA. The layout is performed by RF cadence design system software. The proposed concurrent dual-band LNA occupies an area of 1.0 x 0.84 mm^2, including RF and DC pads.

Table I presents a summary performance of proposed LNA with recently published paper at K-bands using SiGe BiCMOS technology. It is seen that the simulated performance of this work has the best FOM. A large difference FOM comparing to the other works gives a confidence that the measurement performance after device fabrication also has better performance.

Table 1. Summary performance of proposed LNA with recently published paper Waveform

	Tech. (BiCMOS)	Fc (GHz)	Gain (dB)	BW (GHz)	NF (dB)	Pdc (mW)	IIP3 (dBm)	FOM*
Proposed		15	27.5	4	2.4		-16.5	38
LNA	0.13-µm	30	22.8	9	3.2	15.2	-8.4	21
[1]		13.5	22.4	4	3.4		-13.5	7
	0.18-µm	35	20.2	6.4	3.7	36	-16.1	4
[4]		24	21.9	7.7	5.1	-	-10.4	-
	0.18-µm	35	16.6	8.8	7.2	-	-8.3	-
[5]	0.18-µm	27.5	12	9	4.5 6.5	13	-5.3	7
[6]	0.13-µm	33	23.5	1	2.6 3.2	11	-19.5	3
[7]	0.25-µm	30	12.4	6	2	98	-1.3	3

**FOM = Gain (abs) x BW (GHz) / (NF-1) x Fc (GHz) x Pdc (mW)x100 [6]*

4. Conclusion

The aim of this study is to demonstrate the signal processing design of PPG by employing analog Butterworth filter in the open-source software LTspice. From the simulation results, it can be observed that the use of a higher order will yield a smaller Signal-to-Noise Ratio (SNR).

In conclusion, LTspice emerges as a remarkably versatile and powerful tool for analog signal processing within the biomedical domain. Its user-friendly interface facilitates a seamless integration of complex circuit simulations, making it a highly accessible resource for analog circuit designers in the field of biomedical signal processing. The software's simplicity, coupled with its robust capabilities, provides an efficient platform for conceptualizing, implementing, and evaluating intricate analog circuits. The ease of use of LTspice significantly expedites the design process, allowing researchers and engineers to focus on refining and optimizing circuitry for enhanced biomedical signal acquisition and processing. The utility of LTspice extends beyond its simplicity, as it proves to be an invaluable asset for achieving optimal outcomes in the challenging realm of analog signal processing for biomedical applications.

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